

THE SEEBECK EFFECT IN SILICON ICs*

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Abstract

The Seebeck effect in silicon is investigated to evaluate its usefulness for an integrated temperature difference sensor. The theory of the Seebeck effect is briefly explained and some details of the integrated thermopile, the device exploiting the Seebeck effect, are discussed. The experimental results of the measurements are presented, and the maximum attainable sensitivity, which appears to be of the order of 5 to 50 mV/K for thermopiles with internal resistances of 2 k Ω to 200 k Ω , is calculated. It is concluded that the absence of offset, the high sensitivity and the wide operational temperature range make the thermopile a very valuable transducer.

Introduction

One of the promising physical effects that can be exploited in a sensor is the Seebeck effect, in which a temperature difference is converted into an electric voltage [1]. It has the advantage of being a self-generating effect, so that it is without offset, insensitive to interference from sources other than radiation and needs no external power supply. However, the internal resistance can in some cases be rather high, and the required area is relatively large. Even so, it is believed that for temperature-difference measurement the Seebeck sensor can successfully compete with a transistor pair. Useful applications are foreseen in the infrared sensor [2], the flow sensor [3] and the true r.m.s. convertor [4].

Theory

The phenomenon in which a temperature gradient present in a (semi)-conductor induces a gradient in the Fermi energy level is called the Seebeck effect. The following relation applies:

$$\nabla E_F/q = \alpha_s \nabla T \quad (1)$$

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with α_s as the Seebeck coefficient. For non-degenerate silicon, α_s can be calculated by differentiating E_F with respect to the absolute temperature, where E_F is given by

$$E_F = E_c - kT \ln N_c/n \tag{2}$$

For extrinsic n-type silicon, two contributions to α_s can be distinguished (see Fig. 1): $\alpha_{s, E_F - E_c}$, due to a change in the Fermi-Dirac distribution function, and α_{s, E_c} , due to a change in the absolute value of E_c . This is a result of an internal electric field E induced by net diffusion currents and by phonon-drag currents.

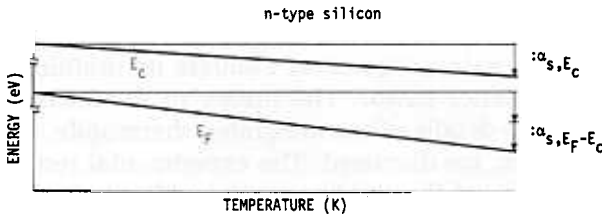


Fig. 1. The variation of E_F due to ∇T .

The first contribution is found by differentiating eqn. (2) with respect to the temperature. The second is found by setting the steady-state net current in the silicon equal to zero:

$$\alpha_{s, E_c} = E/\nabla T \tag{3}$$

$$J_n = \sigma_n E + q \frac{\partial}{\partial T} (D_n \cdot n) \nabla T + qn\phi_n \nabla T = 0 \tag{4}$$

with D_n as the diffusion coefficient. The last term in eqn. (4) represents the phonon-drag current, which is a result of a net current of phonons flowing towards the cold end of the silicon, pulling the charge carriers along with them. The calculations lead to the following equations for extrinsic non-degenerate n-type and p-type silicon:

$$\alpha_s = -\frac{k}{q} \{ \ln N_c/n + 2\frac{1}{2} + r_n \} + \phi_n/\mu_n \quad \text{n-type} \tag{5}$$

$$\alpha_s = \frac{k}{q} \{ \ln N_v/p + 2\frac{1}{2} + r_p \} + \phi_p/\mu_p \quad \text{p-type} \tag{6}$$

where N_c and N_v are the effective densities of states and μ_n and μ_p are taken proportional to the absolute temperature to the power r_n and r_p , respectively. In the literature slightly different expressions for α_s are found. The exponent r which gives the relation between the mobility and the temperature is replaced by the exponent s which gives the relation between the mobility and the energy. For some electron scattering mechanisms these exponents are not the same. However, because the derivation leading to this

more exact formula is more complex, this oversimplification has been made.

Figure 2 shows the Seebeck coefficients at room temperature measured by Geballe and Hull [5] and others [1, 4, 6]. The dotted line indicates the theoretical value of α_s without the phonon-drag contribution.

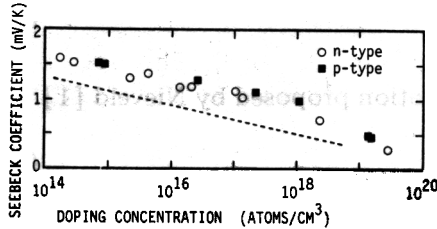


Fig. 2. The Seebeck coefficient of silicon at room temperature as a function of the doping concentration.

Inhomogeneity effects

It is evident from Fig. 2 that the Seebeck coefficient depends strongly on the impurity concentration. In planar IC technology strips made by diffusion or ion-implantation techniques show an inhomogeneous doping profile, which means that they in fact consist of an infinite number of layers, each having a different Seebeck coefficient and internal resistance (see Fig. 3(a)).

In the presence of a temperature gradient the induced Seebeck voltages will even out to the effective Seebeck voltage as the result of equalizing electrical currents. The following equations can be formed:

$$\int_0^{d_j} \mathbf{J}(r) \cdot \mathbf{i}_z \, dr = \int_0^{d_j} \sigma(r) \{ \alpha_s(r) - \alpha_{s,eff} \} \nabla T \cdot \mathbf{i}_z \, dr = 0 \quad (7)$$

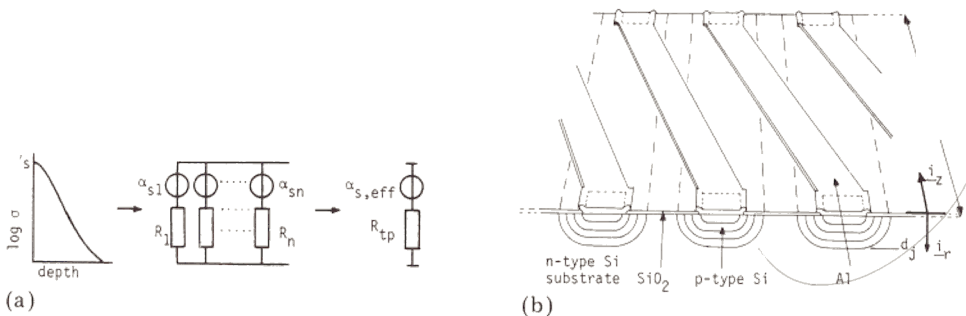


Fig. 3. (a) The equivalent circuit representing the Seebeck effect in an inhomogeneously doped strip. (b) A schematic drawing of a thermopile.

with d_j as the strip depth, $\alpha_{s, \text{eff}}$ as the effective Seebeck coefficient, $\sigma(r)$ as the depth-dependent strip conductivity ($\sigma(r)$ is thought to depend on depth only; for a two-dimensional analysis taking edge effects into account see [7]) and i_z is the unity vector in the z -direction (see Fig. 3(b));

$$\int_0^{d_j} \sigma(r) \alpha_s(r) dr \Big/ \int_0^{d_j} \sigma(r) dr \quad (8)$$

With the aid of the very useful empirical relation proposed by Nieveld [1]:

$$\frac{mk}{q} \ln \{ \sigma_0 / \sigma(r) \} \quad (9)$$

with $m = 2$ and $\sigma_0 = 3.1 \times 10^5$ S/m, it is found that the effective Seebeck coefficient is equal to the coefficient for the surface layer plus a correction factor dependent on the shape of the conductivity profile only. For a Gaussian conductivity profile, with $\sigma(r) = \sigma_s \exp(-0.5(r/r_0)^2)$, the effective Seebeck coefficient equals that of silicon with a conductivity 0.6 times that of the surface layer. Because the shape of the conductivity profile changes only very slowly with temperature, we can hardly distinguish between measuring inhomogeneously doped strips and homogeneous material of the conductivity indicated above.

Experimental results

The IC designed for the experiments (see Fig. 4) was fabricated at the University's IC workshop and consisted primarily of: a large resistor, 5.4 mm wide and 0.3 mm high, to dissipate the power needed for creating a tempera-

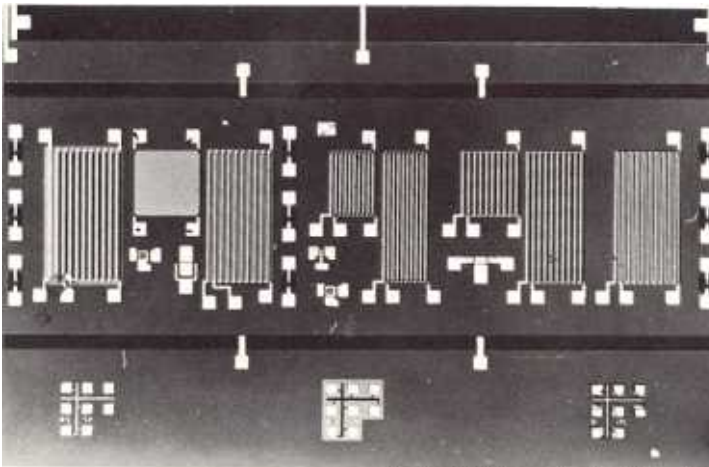


Fig. 4. The IC used to measure the Seebeck coefficient of silicon.

ture gradient in the thermopiles beneath it; seven thermopiles each consisting of 10 silicon strips, interconnected by 10 aluminium strips, to get a tenfold output voltage (as the Seebeck coefficient of aluminium is negligible, no error arises from this set-up); and three sets of three diodes placed at both sides and near the middle of the IC, to measure the temperature difference created over the thermopile ends.

Several different types of thermopiles were tested. The thermopile on the left consisted of 10 shallow n-type strips of the standard emitter (SN) diffusion, each $20\ \mu\text{m}$ wide and 1 mm long, placed in a p-type island to isolate the n-type strips from each other. The thermopile internal resistance, R_{tp} , amounted to approximately 3 k Ω . The thermopile next to that was made of 10 shallow p-type strips of the standard base (SP) diffusion, also $20\ \mu\text{m}$ wide and 1 mm long, yielding an internal resistance R_{tp} of approximately 100 k Ω . Next to that were five thermopiles fabricated with ion implantation, differing only in their geometrical lay-out. Their internal resistances R_{tp} ranged from approximately 2000 times the sheet resistance R_s for $5\ \mu\text{m} \times 1\ \text{mm}$ strips, to 1000 times R_s for $5\ \mu\text{m} \times 0.5\ \text{mm}$ and $10\ \mu\text{m} \times 1\ \text{mm}$ strips and to 500 times R_s for $10\ \mu\text{m} \times 0.5\ \text{mm}$ and $20\ \mu\text{m} \times 1\ \text{mm}$ strips.

Several wafers were processed to get different implantation doses. Measurements were done on samples fabricated according to the following process. The starting material was n-type <100> 5 $\Omega\ \text{cm}$ wafers, in which the SP-diffusion was performed without previous epilayer growth. After the SN deposition and a shortened SN drive-in step of 30 minutes at 1000 $^\circ\text{C}$, implantation windows were etched and subsequently oxidized in dry O_2 for 30 minutes at 1000 $^\circ\text{C}$, creating a protective oxide layer approximately 40 nm thick. Then a boron implantation with dose-energy combinations of $10^{13}/\text{cm}^2$ -150 keV (type H), $10^{14}/\text{cm}^2$ -100 keV (K) and $10^{15}/\text{cm}^2$ -100 keV (P) was carried out, followed by annealing in N_2 ambient at 1000 $^\circ\text{C}$ for 30 minutes. The sheet resistances R_s , calculated with SUPREM II [8], were 2281 Ω , 496 Ω and 109 Ω for the three listed implantations, respectively. Measurements on batches of 24 ICs resulted in R_s values of 2500 Ω , 528 Ω and 90.6 Ω and standard deviations in R_s of 50 Ω , 7 Ω and 0.5 Ω , respectively. The first two values agree rather well with the calculations, bearing in mind that SUPREM II does not take depletion layers into account. The last value is rather low, which is possibly due to a higher mobility.

From the doping profiles calculated by SUPREM II the effective doping concentrations were evaluated for the P, K, H and SP samples. The following values were found for $T = 300\ \text{K}$: $P = 1.7 \times 10^{19}/\text{cm}^3$, $K = 1.8 \times 10^{18}/\text{cm}^3$, $H = 1.7 \times 10^{17}/\text{cm}^3$ and $SP = 1.2 \times 10^{18}/\text{cm}^3$. For the SN sample no calculation can be made because both the doping profile and the behaviour of α_s at very high doping levels ($>10^{20}/\text{cm}^3$) are not well known. The actual determination of α_s was done in two different ways to ensure that no systematic measurement errors were made. First some single ICs were die-bonded in a 24 pin dil ceramic housing with thermally-conducting epo-tek. Upon heating with the heating resistor a temperature difference occurred

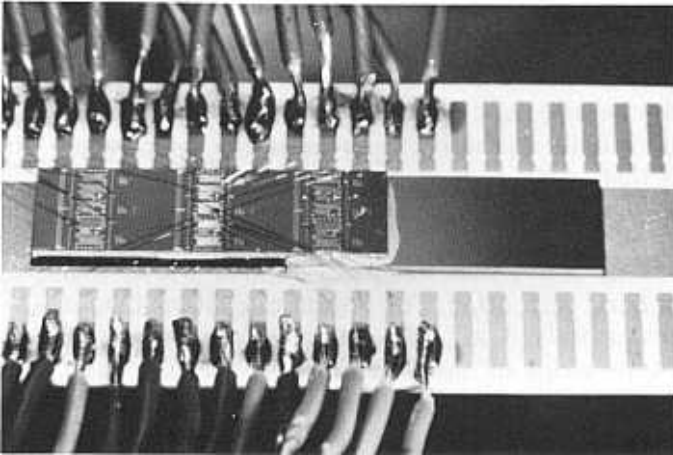


Fig. 5. The 'springboard' die-bonding arrangement of a triple-IC chip.

over the thermopiles, resulting in a thermovoltage. This voltage was measured with a multimeter and divided by the temperature difference as measured with the calibrated diodes. Later a few samples were prepared in which a chip 5.5 mm by 16.5 mm, containing three ICs in a row, was die-bonded at one end on to another piece of silicon, which was die-bonded on a ceramic substrate (see Fig. 5).

In this way a sort of 'springboard' arrangement resulted, in which the heating takes place in the IC at the tip of the 'springboard'. Because the air gap under the free hanging part of the chip does not conduct heat, all the dissipated heat flows through the middle IC, where the Seebeck coefficient was measured, to the right IC, where the thermal connection to the ceramic substrate and the ambient is made. The outcome of the measurements is shown in Figs. 6 and 7. Figure 6 shows the calculated α_s as a function of the temperature. The lines representing the measurements at the 'dil' samples cease at the temperatures where a sharp decrease in the measured α_s started to occur. This is due to leakage currents flowing through the thermopile-substrate junctions, which divide the true Seebeck voltage over the internal resistance and the junction resistance. Because only the latter part is measured, an error is introduced when the thermopile-substrate junction leaks. As the p-n junction resistance falls exponentially with temperature, this effect occurs at a fairly well-defined temperature.

The points that represent measurements on the 'springboard' samples are accurate up to a much higher temperature, because these measurements were carried out on one single strip of each thermopile. This offers the advantage of a tenfold decrease in both the internal resistance and the parasitic junction parallel conduction. In Fig. 7 the Seebeck coefficient of silicon at room temperature is shown as a function of the resistivity. A good agreement exists between previous measurements and the new measure-

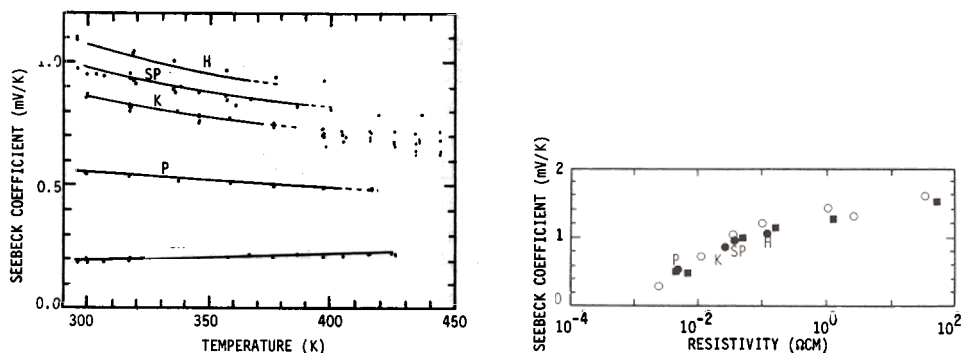


Fig. 6. The Seebeck coefficient of silicon as a function of temperature. The lines represent the measurements on 'dil' samples, the points measurements on 'springboard' samples.

Fig. 7. The Seebeck coefficient of silicon at room temperature as a function of the electrical resistivity. \circ and \blacksquare represent previously reported n-type and p-type points respectively ([5, 1, 4, 6], see also Fig. 2). \bullet represents the new p-type points.

ments, taking into account the uncertainty with which the mobility of holes in silicon is known. Only the H-type implantation coefficient is relatively low. This may be due to the increased inaccuracy (10% instead of 5% maximum error) arising from the high resistances of these samples. This is also evident in Fig. 6, where a noticeable difference exists between the 'dil' and 'spring board' measurements for the H-type samples. The slope of the curve is the factor m in eqn. (9), while the intercept of the curve's tangent with the ρ -axis gives $\rho_0 (= 1/\sigma_0)$. It can be seen that the values of m and ρ_0 are slightly resistivity dependent. This does not seriously affect the calculations of the previous section as long as the change over a decade of ρ is not too sharp.

Optimization

We can use the data of the previous section to optimize the design of thermopiles for given applications. Relevant boundary conditions are usually the internal resistance R_{tp} of the thermopile and the geometrical dimensions, while the main aim is to maximize the sensitivity. This means maximization of the product $\alpha_s N = S(\text{sensitivity})$, where N is the number of strips of the thermopile. In first approximation N is given by the formula

$$R_{tp} = NLNR_s \quad (10)$$

where R_s is the sheet resistance of the thermostrips, L the ratio of the length l and the width w of the thermopile and LNR_s the resistance of one strip. This yields the sensitivity

$$S = \alpha_s (R_{tp}/LR_s)^{1/2} \quad (11)$$

Although S can conceivably be increased infinitely by decreasing L , this will not always be advantageous. In most cases the primary signal to be measured is a heat flow, in which case the temperature difference which occurs is proportional to L , making it better to have a large L . Whether L should be made large or small will in general depend on the application. Because both α_s (through eqn. (9)) and R_s (through the strip depth) are related to the resistivity ρ , we can optimize S by setting its derivative with respect to ρ equal to zero, which results in an optimal Seebeck coefficient $\alpha_{s, \text{opt}}$ of 0.35 mV/K and an optimal silicon resistivity ρ_{opt} of $2 \times 10^{-3} \Omega \text{ cm}$. In many cases, however, it is found that a considerable part of the thermopile area is used in the separation between adjacent strips to ensure that no electrical short-circuiting will occur. This will increase the length/width ratio L of the thermopile, as the thermopile length remains l , whereas the effective thermopile width available to be covered with thermostrips decreases from w to $w - Nb$ if b is the required separation between adjacent strips. In this case, because the area used in separation is proportional to N , it is advantageous to use strips of a higher resistivity, thus lowering the number of strips and decreasing the area used for separation. The rise in α_s will compensate for the loss of strips. In particular, if the separation between adjacent strips is proportional to the strip depth, the optimum is

$$\alpha_{s, \text{opt}} = \frac{3mk}{q} = 0.5 \text{ mV/K} \quad \rho_{\text{opt}} = 6 \times 10^{-3} \Omega \text{ cm}$$

Figure 8 gives an indication of the maximum attainable sensitivity as a function of the internal thermopile resistance divided by the thermopile length/width ratio, for several thermopile widths. As the actual maximum will also depend on the available technological process, this can be an indication only, with large deviations (greater than 10 per cent) possible.

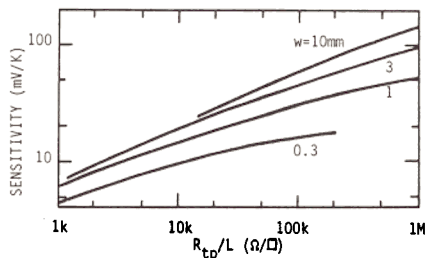


Fig. 8. The optimal attainable thermopile sensitivity as a function of the internal thermopile resistance when using a simple bipolar process.

Conclusions

(a) A good agreement is found between Seebeck coefficients measured with integrated thermopiles made in silicon planar technology and Seebeck coefficients measured with whole silicon crystals.

(b) Thermopiles that work at temperatures up to 180 °C can be fabricated in bipolar technology using standard transistor diffusions. Improvement of the design will probably even increase the maximum operational temperature, while measurement of the short-circuit current could prove a useful alternative in this respect. In that case no leakage through the substrate can occur, as there is no voltage over the thermopile-substrate junctions.

(c) The best compromise between a high thermopile sensitivity and a low thermopile internal resistance is found for silicon having a Seebeck coefficient of 0.35 to 0.5 mV/K and a resistivity of 2 to $6 \times 10^{-3} \Omega \text{ cm}$. With silicon of that resistivity it is feasible to make thermopiles with a sensitivity of 5 to 50 mV/K and an internal resistance of 2 to 200 k Ω .

(d) Compensation of the temperature coefficient of the thermal conductivity of silicon, which is of the order of 0.5%/K at room temperature, with the temperature coefficient of the Seebeck coefficient seems impossible, as the temperature coefficient of α_s of the SP-type, already having an unfavourably high resistivity, is only 0.2%/K. This is disappointing, since in several useful applications of the thermopile a heat flow is the information carrier.

(e) It appears to be possible to make thermopiles with a temperature-independent sensitivity by choosing silicon with a Seebeck coefficient of approximately 350 $\mu\text{V/K}$. This also lies in the range of the optimum choice if a high sensitivity/internal resistance ratio is desired.

On the basis of the material presented here, we can conclude that the Seebeck effect offers the possibility of making temperature difference sensors with very good offset properties and a high accuracy and sensitivity; moreover, these sensors are flexible in design, that is, their size, shape, sensitivity and internal resistance can be chosen to match the demands.

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Biography

Sander van Herwaarden was born in Rotterdam, The Netherlands, in 1957. In 1982 he received the B.Sc. degree in economics from the Erasmus University, Rotterdam, The Netherlands, and in 1983 the M.Sc. degree in Electrical Engineering from the Delft University of Technology. He is currently working towards his Ph.D. on the applications of the silicon thermopile with the sensor group of the Electronic Instrumentation Laboratory.